## DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC


## HEF4534B <br> LSI <br> Real time 5-decade counter

Product specification
File under Integrated Circuits, IC04

PHILIPS

## DESCRIPTION

The HEF4534B is a 5 -decade ripple counter. The binary outputs of the decade counters are time-multiplexed by an internal scanner on four BCD outputs $\left(\mathrm{O}_{0}\right.$ to $\left.\mathrm{O}_{3}\right)$. The selected decade is indicated by a logic HIGH on the appropriate digit select output ( $\mathrm{OS}_{0}$ : units, $1 ; \mathrm{OS}_{1}$ : tens, $10 ; \mathrm{OS}_{2}$ : hundreds, $10^{2} ; \mathrm{OS}_{3}$ : thousands, $10^{3} ; \mathrm{OS}_{4}$ : ten thousands, $10^{4}$ ).

The binary outputs ( $\mathrm{O}_{0}$ to $\mathrm{O}_{3}$ ) and the select outputs $\left(\mathrm{OS}_{0}\right.$ to $\left.\mathrm{OS}_{4}\right)$ are 3-state controlled via enable inputs $\overline{\mathrm{EO}}$ and $\overline{\mathrm{EOS}}$ respectively, allowing interface with other bus orientated devices. Cascading may be accomplished by using the carry out (TC). The counter is triggered by a LOW to HIGH transition on the decade clock (CPA) and is reset by a HIGH level on the master reset (MR). The
scanner is triggered by a LOW to HIGH transition on the scanner clock (CPS) and is reset (select ten thousand counter) by a HIGH level on the scanner reset ( $\mathrm{MR}_{\mathrm{sc}}$ ).

The counter can operate in four modes depending on the state of the mode select inputs $\left(\mathrm{S}_{\mathrm{A}}, \mathrm{S}_{\mathrm{B}}\right)$. The error detector will detect an error when a positive edge on CPA is not accompanied by a negative edge on the error detector clock $\overline{\text { CPE }}$ or vice versa, within time limits adjusted by external capacitors connected to $\mathrm{C}_{\text {ext } 1}$ and $\mathrm{C}_{\text {ext } 2 \text {. Three or }}$ more detected errors result in a HIGH level on the error output (OER). The error detector is reset by a HIGH level on MR.

Schmitt-trigger action in the clock inputs makes the circuit highly tolerant to slower clock rise and fall times.

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Fig. 1 Pinning diagram.
$\begin{array}{ll}\text { HEF4534BP(N): } & \text { 24-lead DIL; plastic (SOT101-1) } \\ \text { HEF4534BD(F): } & \text { 24-lead DIL; ceramic (cerdip) (SOT94) } \\ \text { HEF4534BT(D): } & \text { 24-lead SO; plastic (SOT137-1) }\end{array}$
( ): Package Designator North America

## PINNING

| $\mathrm{O}_{1}$ to $\mathrm{O}_{3}$ | BCD outputs |
| :--- | :--- |
| $\mathrm{OS}_{0}$ to $\mathrm{OS}_{3}$ | digit select outputs |
| OER | error output |
| CPA | decade clock input |
| CPS | scanner clock input |
| $\overline{\mathrm{CPE}}$ | error detector clock input |
| $\mathrm{S}_{\mathrm{A}}, \mathrm{S}_{\mathrm{B}}$ | mode select inputs |
| $M R$ | master reset input |
| $\mathrm{MR}_{\text {sc }}$ | scanner reset input |
| TC | carry out |

FAMILY DATA, IDD LIMITS category LSI
See Family Specifications


Fig. 2 Functional block diagram.
$\qquad$

MODE CONTROL FUNCTION TABLE

| SELECT INPUTS |  | 1ST DECADE OUTPUT | CARRY TO 2ND STAGE | CARRY TO 4TH STAGE | MODE |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{S}_{\text {A }}$ | $\mathrm{S}_{\mathrm{B}}$ |  |  |  |  |
| L | L | normal count and display | at 9 to 0 transition of the 1st decade | at 9 to 0 transition of the 3rd decade | 5-decade counter |
| L | H | inhibited | input clock | input clock | test purposes: clock directly into stages 1, 2 and 4 |
| H | H | inhibited | at 4 to 5 transition of the 1 st decade | at 9 to 0 transition of the 3rd decade | 4-decade counter with $\div 10$ and roundoff at front end |
| H | L | display counts: $\begin{aligned} & 3,4,5,6,7=5 \\ & 8,9,0,1,2=0 \end{aligned}$ | at 7 to 8 transition of the 1 st decade | at 9 to 0 transition of the 3rd decade | 4-decade counter; $1 / 2$-pence capability |



The skew time is the time difference between the LOW to HIGH transition of CPA and the HIGH to LOW transition of $\overline{\mathrm{CPE}}$ or vice versa (see Fig.4). The skew time is typically proportional to the external capacitor ( $\mathrm{C}_{\text {ext }}$ ) connected from $\mathrm{C}_{\text {ext1 }}$ and $\mathrm{C}_{\text {ext2 }}$ (pins 1 and 22) to $\mathrm{V}_{\mathrm{SS}}$. The error detector will count an error when a positive edge on the counter clock CPA is not succeeded by a negative edge on
the error detector clock $\overline{\text { CPE }}$ within a skew time $\mathrm{t}_{\mathrm{SK} 1}$ (adjustable by $\mathrm{C}_{\mathrm{ext1}}$ at pin 1). The same holds for a negative edge at CPE succeeded by a positive on CPA within a skew time $\mathrm{t}_{\mathrm{SK} 2}$ (adjustable by $\mathrm{C}_{\text {ext2 }}$ at pin 22). If error detection is not needed, $\overline{\text { CPE must be either HIGH or }}$ LOW and no $\mathrm{C}_{\text {ext }}$ is applied. For further information see Fig.5.

Fig. 4 Skew times timing diagram; $\mathrm{t}_{\text {WCPA }}>\mathrm{t}_{\mathrm{SK} 1}$; $t_{\text {WCPE }}>t_{\text {SK2 }}$.



Note 1: Skew in this area results in counted error.
Note 2: Skew in the area between max. and min. curves may or may not result in counted error.
Note 3: Skew in this area results in no error counted.
Fig. 5 Typical clock skew as a function of the supply voltage. This graph is accurate for $C_{\text {ext }} \geq 100 \mathrm{pF}$ and $\mathrm{T}_{\mathrm{amb}}=25^{\circ} \mathrm{C}$.


Fig. 6 Carry timing diagram.
LSI


Note: If $\mathrm{S}_{\mathrm{B}}=\mathrm{H}$, the 1st decade is inhibited and the cycle will be shortened to four stages (see dotted lines).
Fig. 7 Scanner timing diagram.


Fig. 8 Counter timing diagram.

## AC CHARACTERISTICS

$\mathrm{V}_{\mathrm{SS}}=0 \mathrm{~V} ; \mathrm{T}_{\mathrm{amb}}=25^{\circ} \mathrm{C} ; \mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}$; input transition times $\leq 20 \mathrm{~ns}$

|  | $\mathrm{V}_{\mathrm{DD}}$ V | SYMBOL | MIN. TYP. | MAX. |  | TYPICAL EXTRAPOLATION FORMULA |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Propagation delays $\mathrm{CPA} \rightarrow \mathrm{O}_{\mathrm{n}}$ <br> D1 selected <br> HIGH to LOW <br> LOW to HIGH | $\begin{array}{r} 5 \\ 10 \\ 15 \end{array}$ | $\mathrm{t}_{\text {PHL }}$ | $\begin{array}{r} 300 \\ 130 \\ 95 \end{array}$ | $\begin{aligned} & 600 \\ & 260 \\ & 190 \end{aligned}$ | ns <br> ns ns | $\begin{array}{r} 283 \mathrm{~ns}+(0,55 \mathrm{~ns} / \mathrm{pF}) \mathrm{C}_{\mathrm{L}} \\ 119 \mathrm{~ns}+(0,23 \mathrm{~ns} / \mathrm{pF}) \mathrm{C}_{\mathrm{L}} \\ 87 \mathrm{~ns}+(0,16 \mathrm{~ns} / \mathrm{pF}) \mathrm{C}_{\mathrm{L}} \end{array}$ |
|  | $\begin{array}{r} 5 \\ 10 \\ 15 \end{array}$ | $\mathrm{t}_{\text {PLH }}$ | $\begin{array}{r} 240 \\ 100 \\ 75 \end{array}$ | $\begin{aligned} & \hline 480 \\ & 200 \\ & 150 \end{aligned}$ | ns <br> ns <br> ns | $\begin{array}{r} \hline 213 \mathrm{~ns}+(0,55 \mathrm{~ns} / \mathrm{pF}) \mathrm{C}_{\mathrm{L}} \\ 89 \mathrm{~ns}+(0,23 \mathrm{~ns} / \mathrm{pF}) \mathrm{C}_{\mathrm{L}} \\ 67 \mathrm{~ns}+(0,16 \mathrm{~ns} / \mathrm{pF}) \mathrm{C}_{\mathrm{L}} \end{array}$ |
| $\mathrm{CPA} \rightarrow \mathrm{O}_{\mathrm{n}}$ <br> D5 selected <br> HIGH to LOW | $\begin{array}{r} 5 \\ 10 \\ 15 \end{array}$ | $\mathrm{t}_{\text {PHL }}$ | $\begin{aligned} & 550 \\ & 230 \\ & 170 \end{aligned}$ | $\begin{array}{r} 1100 \\ 460 \\ 340 \end{array}$ | ns <br> ns <br> ns | $\begin{aligned} & 523 \mathrm{~ns}+(0,55 \mathrm{~ns} / \mathrm{pF}) \mathrm{C}_{\mathrm{L}} \\ & 219 \mathrm{~ns}+(0,23 \mathrm{~ns} / \mathrm{pF}) \mathrm{C}_{\mathrm{L}} \\ & 162 \mathrm{~ns}+(0,16 \mathrm{~ns} / \mathrm{pF}) \mathrm{C}_{\mathrm{L}} \\ & \hline \end{aligned}$ |
| LOW to HIGH | $\begin{array}{r} 5 \\ 10 \\ 15 \end{array}$ | tpLH | $\begin{aligned} & 550 \\ & 230 \\ & 170 \end{aligned}$ | $\begin{array}{r} 1100 \\ 460 \\ 340 \end{array}$ | ns <br> ns <br> ns | $\begin{aligned} & 523 \mathrm{~ns}+(0,55 \mathrm{~ns} / \mathrm{pF}) \mathrm{C}_{\mathrm{L}} \\ & 219 \mathrm{~ns}+(0,23 \mathrm{~ns} / \mathrm{pF}) \mathrm{C}_{\mathrm{L}} \\ & 162 \mathrm{~ns}+(0,16 \mathrm{~ns} / \mathrm{pF}) \mathrm{C}_{\mathrm{L}} \\ & \hline \end{aligned}$ |
| $\mathrm{CPA} \rightarrow \mathrm{TC}$ <br> LOW to HIGH | $\begin{array}{r} 5 \\ 10 \\ 15 \end{array}$ | $\mathrm{t}_{\text {PLH }}$ | $\begin{aligned} & \hline 420 \\ & 190 \\ & 140 \end{aligned}$ | $\begin{aligned} & \hline 840 \\ & 380 \\ & 280 \end{aligned}$ | ns <br> ns ns | $\begin{aligned} & \hline 393 \mathrm{~ns}+(0,55 \mathrm{~ns} / \mathrm{pF}) \mathrm{C}_{\mathrm{L}} \\ & 179 \mathrm{~ns}+(0,23 \mathrm{~ns} / \mathrm{pF}) \mathrm{C}_{\mathrm{L}} \\ & 132 \mathrm{~ns}+(0,16 \mathrm{~ns} / \mathrm{pF}) \mathrm{C}_{\mathrm{L}} \end{aligned}$ |
| $\mathrm{MR} \rightarrow \mathrm{O}_{\mathrm{n}}$ <br> HIGH to LOW | $\begin{array}{r} 5 \\ 10 \\ 15 \end{array}$ | $\mathrm{t}_{\text {PHL }}$ | $\begin{array}{r} 200 \\ 85 \\ 60 \end{array}$ | $\begin{aligned} & 400 \\ & 170 \\ & 120 \end{aligned}$ | ns <br> ns ns | $\begin{aligned} 173 \mathrm{~ns} & +(0,55 \mathrm{~ns} / \mathrm{pF}) \mathrm{C}_{\mathrm{L}} \\ 74 \mathrm{~ns} & +(0,23 \mathrm{~ns} / \mathrm{pF}) \mathrm{C}_{\mathrm{L}} \\ 52 \mathrm{~ns} & +(0,16 \mathrm{~ns} / \mathrm{pF}) \mathrm{C}_{\mathrm{L}} \end{aligned}$ |
| $\text { MR } \rightarrow \text { OER }$ <br> HIGH to LOW | $\begin{array}{r} 5 \\ 10 \\ 15 \end{array}$ | $\mathrm{t}_{\text {PHL }}$ | $\begin{array}{r} 140 \\ 65 \\ 50 \end{array}$ | $\begin{aligned} & 280 \\ & 130 \\ & 100 \end{aligned}$ | ns <br> ns <br> ns | $\begin{aligned} 113 \mathrm{~ns} & +(0,55 \mathrm{~ns} / \mathrm{pF}) \mathrm{C}_{\mathrm{L}} \\ 54 \mathrm{~ns} & +(0,23 \mathrm{~ns} / \mathrm{pF}) \mathrm{C}_{\mathrm{L}} \\ 42 \mathrm{~ns} & +(0,16 \mathrm{~ns} / \mathrm{pF}) \mathrm{C}_{\mathrm{L}} \end{aligned}$ |
| $\mathrm{CPS} \rightarrow \mathrm{O}_{\mathrm{n}}$ <br> HIGH to LOW | $\begin{array}{r} 5 \\ 10 \\ 15 \end{array}$ | $\mathrm{t}_{\text {PHL }}$ | $\begin{array}{r} \hline 225 \\ 95 \\ 70 \end{array}$ | $\begin{aligned} & \hline 450 \\ & 190 \\ & 140 \end{aligned}$ | ns <br> ns <br> ns | $\begin{array}{r} \hline 198 \mathrm{~ns}+(0,55 \mathrm{~ns} / \mathrm{pF}) \mathrm{C}_{\mathrm{L}} \\ 84 \mathrm{~ns}+(0,23 \mathrm{~ns} / \mathrm{pF}) \mathrm{C}_{\mathrm{L}} \\ 62 \mathrm{~ns}+(0,16 \mathrm{~ns} / \mathrm{pF}) \mathrm{C}_{\mathrm{L}} \end{array}$ |
| LOW to HIGH | $\begin{array}{r} 5 \\ 10 \\ 15 \end{array}$ | tple | $\begin{array}{r} 225 \\ 95 \\ 70 \end{array}$ | $\begin{aligned} & 450 \\ & 190 \\ & 140 \end{aligned}$ | ns <br> ns <br> ns | $\begin{array}{r} 198 \mathrm{~ns}+(0,55 \mathrm{~ns} / \mathrm{pF}) \mathrm{C}_{\mathrm{L}} \\ 84 \mathrm{~ns}+(0,23 \mathrm{~ns} / \mathrm{pF}) \mathrm{C}_{\mathrm{L}} \\ 62 \mathrm{~ns}+(0,16 \mathrm{~ns} / \mathrm{pF}) \mathrm{C}_{\mathrm{L}} \end{array}$ |
| $\mathrm{CPS} \rightarrow \mathrm{OS}_{\mathrm{n}}$ <br> HIGH to LOW | $\begin{array}{r} 5 \\ 10 \\ 15 \end{array}$ | $\mathrm{t}_{\text {PHL }}$ | $\begin{array}{r} 170 \\ 70 \\ 50 \end{array}$ | $\begin{aligned} & 340 \\ & 140 \\ & 100 \end{aligned}$ | ns ns ns | $\begin{array}{r} 143 \mathrm{~ns}+(0,55 \mathrm{~ns} / \mathrm{pF}) \mathrm{C}_{\mathrm{L}} \\ 59 \mathrm{~ns}+(0,23 \mathrm{~ns} / \mathrm{pF}) \mathrm{C}_{\mathrm{L}} \\ 42 \mathrm{~ns}+(0,16 \mathrm{~ns} / \mathrm{pF}) \mathrm{C}_{\mathrm{L}} \end{array}$ |
| $\mathrm{CPS} \rightarrow \mathrm{OS}_{\mathrm{n}}$ <br> LOW to HIGH | $\begin{array}{r} 5 \\ 10 \\ 15 \end{array}$ | $\mathrm{t}_{\text {PLH }}$ | $\begin{array}{r} \hline 170 \\ 70 \\ 50 \end{array}$ | $\begin{aligned} & 340 \\ & 140 \\ & 100 \end{aligned}$ | ns ns ns | $\begin{array}{r} 143 \mathrm{~ns}+(0,55 \mathrm{~ns} / \mathrm{pF}) \mathrm{C}_{\mathrm{L}} \\ 59 \mathrm{~ns}+(0,23 \mathrm{~ns} / \mathrm{pF}) \mathrm{C}_{\mathrm{L}} \\ 42 \mathrm{~ns}+(0,16 \mathrm{~ns} / \mathrm{pF}) \mathrm{C}_{\mathrm{L}} \end{array}$ |

Real time 5-decade counter

|  | $\mathbf{V}_{\mathbf{D D}}$ |  | SYMBOL | MIN. | TYP. | MAX. |
| :---: | ---: | :--- | ---: | ---: | ---: | ---: |\(\left.\quad \begin{array}{c}TYPICAL EXTRAPOLATION <br>

FORMULA\end{array}\right]\)

## AC CHARACTERISTICS

$\mathrm{V}_{\mathrm{SS}}=0 \mathrm{~V} ; \mathrm{T}_{\mathrm{amb}}=25^{\circ} \mathrm{C} ; \mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}$; input transition times $\leq 20 \mathrm{~ns}$


|  | $\mathbf{V}_{\mathbf{D D}}$ | SYMBOL | MIN. | TYP. | MAX. |  |
| :--- | ---: | :--- | ---: | ---: | ---: | ---: |
|  |  |  |  |  |  |  |
|  | $\mathbf{V}$ | 5 |  | 2,5 | 5 | MHz |
| Maximum clock | 10 | $\mathrm{f}_{\text {max }}$ | 6 | 12 | MHz |  |
| pulse frequency | 15 |  | 8 | 16 | MHz |  |
| CPA and CPS |  |  |  |  |  |  |


|  | $\mathrm{V}_{\mathrm{DD}}$ V | TYPICAL FORMULA FOR P ( $\mu \mathrm{W}$ ) |  |
| :---: | :---: | :---: | :---: |
| Dynamic power dissipation per package (P) ${ }^{(1)}$ | $\begin{array}{r} 5 \\ 10 \\ 15 \end{array}$ | $\begin{array}{r} 1100 f_{i}+\sum\left(f_{0} C_{L}\right) \times V_{D D^{2}} \\ 4800 f_{i}+\sum\left(f_{o} C_{L}\right) \times V_{D D^{2}} \\ 12000 f_{i}+\sum\left(f_{o} C_{L}\right) \times V_{D D^{2}} \end{array}$ | where <br> $\mathrm{f}_{\mathrm{i}}=$ input freq. $(\mathrm{MHz})$ <br> $\mathrm{f}_{\mathrm{o}}=$ output freq. $(\mathrm{MHz})$ <br> $\mathrm{C}_{\mathrm{L}}=$ load cap. $(\mathrm{pF})$ <br> $\sum\left(\mathrm{f}_{0} \mathrm{C}_{\mathrm{L}}\right)=$ sum of outputs <br> $\mathrm{V}_{\mathrm{DD}}=$ supply voltage ( V ) |

## Note

1. $\mathrm{C}_{\mathrm{ext}}=0$.

## APPLICATION INFORMATION



Fig. 9 Two HEF4534B ICs connected for cascade operation. TC is HIGH for a single clock period when all five BCD decades go to zero. TC also goes HIGH when MR is applied.


Fig. 10 Forcing a decade to the $\mathrm{O}_{\mathrm{n}}$ outputs. When the $\mathrm{O}_{\mathrm{n}}$ outputs of a given decade are required, this configuration will lock-up the selected decade within four clock cycles. The select line feed back may be hardwired or switched.

